Abstracts

Design of a Low Phase Distortion GaAs FET Power Limiter (Short Papers)

T. Parra, M. Gayral, O. Llopis, M. Pouysegur, J.F. Sautereau and J. Graffeuil. "Design of a Low Phase Distortion GaAs FET Power Limiter (Short Papers)." 1991 Transactions on Microwave Theory and Techniques 39.6 (Jun. 1991 [T-MTT]): 1059-1062.

A simple design technique for a GaAs FET limiter exhibiting minimum phase distortion is presented. The key idea in removing phase distotion by selecting an appropriate device and designing a bias circuit is based on the observed properties of the gate barrier under large-signal conditions. Also presented are some illustrative examples and simulation results. The proposed technique is suitable for MMIC design.

❑ Return to main document.